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EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,032	LANDOLT, OLIVER DIETER	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-9 and 12-20* is/are rejected.

7)☒ Claim(s) *3,4,10, and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Note that line 12 recites the limitation " ... of said second output to control ..." and is indefinite because the second output could be from the second memory, the second current source, the second feedback capacitor, or the second output transistor. The examiner interpreted the limitation "the second output" as "the second output transistor".

2. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Note that line 8 recites the limitation "output node" and is indefinite because the output node can be interpreted as the output node of the circuit, an output node of the current, or an output node of the output transistor. The examiner interpreted the limitation "output node" as "the output node of the output transistor"

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1 and 6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Itakura et al. (Pub No.: 2002/0180685) in view of Mortara ("A 12-Transistor PFM Demodulator for Analog Neural Networks Communication" by Alessandro Mortara and Eric A. Vittoz, IEEE Transactions on Neural Networks, Vol. 6, No. 5, September 1995, pp. 1280-1283).

With respect to **Claim 1**, Itakura discloses a driving circuit *(See figure 31)*. Itakura teaches the driving circuit to comprise an output transistor *(Mp43)* connected between a voltage terminal *(Vdd)* and an output node *(node that is common to the resistor Rf and the terminals of Mp43 and Mn43)* to produce an output signal on the output node. Itakura teaches the output transistor to include a control terminal *(the control terminal is connected to a node common to Cf1, where the node connects to the terminal of Mp45)*; a current source *(Ib1)* connected to the control terminal of the output transistor to provide a reference current *(the connection of the current source to the control terminal of the output transistor is either through Mn41 when the switch SW20 is closed or through Mn42)*; and a feedback capacitor *(Cf1)* connected from the output node to the control terminal of the output transistor to control the output transistor as a function of a difference between current through the capacitor and the reference current.

Itakura does not teach the current source being configured to generate the reference current proportional to a reference voltage and a reference frequency.

Mortara teaches a current source being configured to generate a reference current proportional to a reference voltage and a reference frequency *(p 1282, right column under results see second paragraph and third paragraph lines 1-3; p1281, See figure 3, left column third paragraph, lines 1-6; note that in figure 3, parameters of the transistors T3 and T4 were varied*

to obtain the relationship of frequency and current as shown in figure 4; See applicants admission of the teachings of Mortara section [0025] of the specification).

Mortara modifies the circuit of Itakura *(Itakura : See figure 31)* by replacing the current source Ib1 with a demodulator circuit *(Mortara: p 1281, See figure 3)* such that the output current of the demodulator circuit is connected to the wiring common to elements Mn41 and Mn42 of Itakura in figure 31.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a current source being configured to generate a reference current proportional to a reference voltage and a reference frequency, as taught by Mortara, to the driving circuit of Itakura, so as to provide a stable and simple circuit that avoids the difficulty of a large time constant *(p 1283, V1 conclusion; note that figure 4 shows stability since the relationship between frequency and current is linear).*

With respect to **Claim 6**, the driver circuit of Itakura as modified by Mortara in claim 1, teaches the current source includes a frequency-to-current converter *(p 1282, See figure 4 which shows the relationship of frequency and current of the circuit shown in figure 3).*

With respect to **Claim 7**, the driver circuit of claim 1, Itakura teaches a first switch *(See figure 31, Mn41)* located between the voltage terminal and the output transistor *(note that the connection to the output transistor is through the terminal of the output transistor that is common to Cf1 and the output node, designated with a dotted line; the connection to the voltage terminal is through either Mp44 or through both SW20 and Mp45)* and a second switch *(Mn42)*

located between the current source and the control terminal of the output transistor *(note that the connection to the control terminal is the connection area that is common to Mp45, Cf1, SW20 and Mp43)*, the first and second switches being controlled by an input signal *(Itakura notes in the specification that IN+ and IN- are representative of input signals; p. 4, [0065], lines 11-12).*

With respect to **Claim 8**, the driver circuit of Claim 1, Itakura teaches a second output transistor *(Mn43)* connected between the output node *(node that is common to the resistor Rf and the terminals of Mn43 and Mp43)* and a second voltage terminal *(Vss)*, the second output transistor including a control terminal *(the control terminal is connected to a node common to Cf2, where the node connects to the terminal of Mn45)*; a second current source *(Ib2)* connected to the control terminal of the second output transistor *(the connection of the current source to the control terminal of the output transistor is either through Mp41 when the switch SW21 is closed or through Mp42)*; and a second feedback capacitor *(Cf2)* connected from the output node to the control terminal of the second output transistor.

4. **Claims 9 and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Itakura and Chung (Pub. No.: US 2004/0036670).

With respect to **Claim 9**, Itakura discloses a driving circuit *(See figure 31)*. Itakura teaches the driving circuit to comprise an output transistor *(Mp43)* connected between a voltage terminal *(Vdd)* and an output node *(node that is common to the resistor Rf and the terminals of Mp43 and Mn43)* to produce an output signal on the output node. Itakura teaches the output

transistor to include a control terminal *(the control terminal is connected to a node common to Cf1, where the node connects to the terminal of Mp45)*; a current source *(Ib1)* connected to the control terminal of the output transistor to provide a reference current *(the connection of the current source to the control terminal of the output transistor is either through Mn41 when the switch SW20 is closed or through Mn42)*; and a feedback capacitor *(Cf1)* connected from the output node to the control terminal of the output transistor to control a rate of signal change on the output node.

Itakura does not teach a memory connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal from a previous operating cycle in which the output transistor was activated.

Chung teaches a memory *(See figure 11, element 530)* connected to the control terminal of the output transistor *(See figure 11, element 510: driver amplifier; See figure 14: driver amplifier, element 512: driving stage)*, the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated *([0078]; [0080]; [0081])*.

Chung modifies the circuit of Itakura by adding a data latch, a bias control voltage generator *(Chung: See figure 11)*, a switch, and a bias current source *(Chung: See figure 14)* such that the switch and bias current is connected to the node common to elements Mn41 and Mn42 *(Itakura: See figure 31)*. Note that the switch is controlled by outputs of the bias control voltage generator *(Chung: See figure 11)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a memory connected to the control terminal of the output transistor,

the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated, as taught by Chung, to the driver circuit of Itakura, so as to control the slew rate of a driver for reducing power consumption *(Chung: [0090])*.

With respect to **Claim 16**, Itakura teaches a method of driving an electrical device *(See figure 31)*, the method comprising: receiving an input signal *([0113], lines 1-3)*; and controlling *(See figure 31, the capacitor Cf1 controls the output signal)* the output signal on the output node using a difference between a reference current and current capacitively fed back from the output node.

Itakura does not mention applying a stored signal to an output transistor in response to the input signal to produce an output signal on the output node of the output transistor.

Chung teaches a memory *(See figure 11, element 530)* connected to a control terminal of an output transistor *(See figure 11, element 510: driver amplifier; See figure 14: driver amplifier, element 512: driving stage)*, applying a stored signal to an output transistor in response to an input signal to produce an output signal on the output node of the output transistor *([0078]; [0080]; [0081])*.

Chung modifies the circuit of Itakura by adding a data latch, a bias control voltage generator *(Chung: See figure 11)*, a switch, and a bias current source *(Chung: See figure 14)* such that the switch and bias current is connected to the node common to elements Mn41 and Mn42 *(Itakura: See figure 31)*. Note that the switch is controlled by outputs of the bias control voltage generator *(Chung: See figure 11)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a memory connected to the control terminal of the output transistor, and applying a stored signal to an output transistor in response to the input signal to produce an output signal on the output node of the output transistor, as taught by Chung, to the driver circuit of Itakura, so as to control the slew rate of a driver for reducing power consumption *(Chung: [0090])*.

With respect to **Claim 15**, the driver circuit of claim 9, Itakura teaches a second output transistor *(Mn43)* connected between the output node *(node that is common to the resistor Rf and the terminals of Mn43 and Mp43)* and a second voltage terminal *(Vss)*, the second output transistor including a control terminal *(the control terminal is connected to a node common to Cf2, where the node connects to the terminal of Mn45)*; a second current source *(Ib2)* connected to the control terminal of the second output transistor to provide a second reference current *(the connection of the current source to the control terminal of the output transistor is either through Mp41 when the switch SW21 is closed or through Mp42)*; and a second feedback capacitor *(Cf2)* connected from the output node to the control terminal of the second output transistor to control a second rate of signal change on the output node.

Itakura does not teach a second memory connected to the control terminal of the second output transistor, the second memory being configured to store a signal on the control terminal of the second output transistor from a previous operating cycle when the second output transistor was activated.

Please note the above teachings of Chung with respect to a memory.

Chung modifies the circuit of Itakura by adding a data latch, a bias control voltage generator *(Chung: See figure 11)*, a switch, and a bias current source *(Chung: See figure 14)* such that the switch and bias current is connected to the node common to elements Mp41 and Mp42 *(Itakura: See figure 31)*. Note that the switch is controlled by outputs of the bias control voltage generator *(Chung: See figure 11)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a second memory connected to the control terminal of the second output transistor, the second memory being configured to store a signal on the control terminal of the second output transistor from a previous operating cycle when the second output transistor was activated, as taught by Chung, to the driver circuit of Itakura, so as to control the slew rate of a driver for reducing power consumption *(Chung: [0090])*.

With respect to **Claim 17**, the driver circuit of Itakura as modified by Chung in claim 16, teaches, storing a control signal *(See figure 11, the stored signal is equivalent to data relating to the previous operating cycle)* on the output transistor as the stored signal.

5. **Claims 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Itakura and Chung as applied to claim 9 above, and further in view of Mortara.

With respect to **Claim 12**, the driver circuit of claim 9, neither Itakura nor Chung teach the current source is configured to generate a reference current proportional to a reference voltage and a reference frequency.

Mortara teaches a current source being configured to generate a reference current proportional to a reference voltage and a reference frequency *(p 1282, right column under results see second paragraph and third paragraph lines 1-3; p1281, See figure 3, left column third paragraph, lines 1-6; note that in figure 3, parameters of the transistors T3 and T4 were varied to obtain the relationship of frequency and current as shown in figure 4; See applicants admission of the teachings of Mortara section [0025] of the specification).*

Mortara modifies the circuit of Itakura *(Itakura : See figure 31)* by replacing the current source Ib1 with a demodulator circuit *(Mortara: p 1281, See figure 3)* such that the output current of the demodulator circuit is connected to the wiring common to elements Mn41 and Mn42 of Itakura in figure 31.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a current source being configured to generate a reference current proportional to a reference voltage and a reference frequency, as taught by Mortara, to the driving circuit of Itakura as modified by Chung, so as to provide a stable and simple circuit that avoids the difficulty of a large time constant *(p 1283, V1 conclusion; note that figure 4 shows stability since the relationship between frequency and current is linear).*

With respect to **Claim 13**, the driver circuit of Itakura and Chung as modified by Mortara in claim 12, teaches the current source includes a frequency-to-current converter *(p 1282, See figure 4 which shows the relationship of frequency and current of the circuit shown in figure 3).*

With respect to **Claim 14**, the driver circuit of claim 12, Itakura teaches a first switch *(See figure 31, Mn41)* located between the voltage terminal and the output transistor *(note that the connection to the output transistor is through the terminal of the output transistor that is common to Cf1 and the output node, designated with a dotted line; the connection to the voltage terminal is through either Mp44 or through both SW20 and Mp45)* and a second switch *(Mn42)* located between the current source and the control terminal of the output transistor *(note that the connection to the control terminal is the connection area that is common to Mp45, Cf1, SW20 and Mp43)*, the first and second switches being controlled by an input signal *(Itakura notes in the specification that IN+ and IN- are representative of input signals; p. 4, [0065], lines 11-12).*

6. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Itakura and Mortara as applied to claim 1 above, and further in view of Chung.

With respect to **Claim 2**, the driver circuit of claim 1, neither Itakura nor Mortara teach a memory operatively connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated.

Chung teaches a memory *(See figure 11, element 530)* operatively connected to the control terminal of the output transistor *(See figure 11, element 510: driver amplifier; See figure 14: driver amplifier, element 512: driving stage)*, the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated *([0078]; [0080]; [0081])*.

Chung modifies the circuit of Itakura as modified by Mortara by adding a data latch, a bias control voltage generator *(Chung: See figure 11)*, a switch, and a bias current source *(Chung: See figure 14)* such that the switch and bias current is connected to the node common to elements Mn41 and Mn42 *(Itakura: See figure 31)*. Note that the switch is controlled by outputs of the bias control voltage generator *(Chung: See figure 11)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a memory operatively connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated, as taught by Chung, to the driver circuit of Itakura as modified by Mortara, so as to control the slew rate of a driver for reducing power consumption *(Chung: [0090])*.

7. **Claims 18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Itakura and Chung as applied to claim 16 above, and further in view of Mortara.

With respect to **Claim 18**, the method of claim 16, neither Itakura nor Chung teach generating a reference current using a reference frequency and a reference voltage, and applying the reference current to a control terminal of the output transistor.

Mortara teaches a current source being configured to generate a reference current using a reference voltage and a reference frequency *(p 1282, right column under results see second paragraph and third paragraph lines 1-3; p1281, See figure 3, left column third paragraph, lines 1-6; note that in figure 3, parameters of the transistors T3 and T4 were varied to obtain the*

relationship of frequency and current as shown in figure 4; See applicants admission of the teachings of Mortara section [0025] of the specification).

Mortara modifies the circuit of Itakura *(Itakura : See figure 31)* by replacing the current source Ib1 with a demodulator circuit *(Mortara: p 1281, See figure 3)* such that the output current of the demodulator circuit is connected to the wiring common to elements Mn41 and Mn42 of Itakura in figure 31. The modification results in an application of the reference current to a control terminal of the output transistor.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made generate a reference current using a reference frequency and a reference voltage, as taught by Mortara, to the driving circuit of Itakura, so as to provide a stable and simple circuit that avoids the difficulty of a large time constant *(p 1283, V1 conclusion; note that figure 4 shows stability since the relationship between frequency and current is linear).*

With respect to **Claim 19**, the method of claim 16, Itakura teaches controlling *(See figure 31, the capacitor Cf2 controls the output signal)* the output signal on the output node using a difference between a second reference current *(See figure 31, element Ib2)* and a second current capacitively fed back from the output node to the second output transistor.

Itakura does not teach applying a second stored signal to a second output transistor in response to the input signal to change the output signal on the output node.

Please note the above teachings of Chung with respect to a storing a signal in a memory in claim 16.

Chung modifies the circuit of Itakura by adding a data latch, a bias control voltage generator *(Chung: See figure 11)*, a switch, and a bias current source *(Chung: See figure 14)* such that the switch and bias current is connected to the node common to elements Mp41 and Mp42 *(Itakura: See figure 31)*. Note that the switch is controlled by outputs of the bias control voltage generator *(Chung: See figure 11)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a memory connected to the control terminal of the output transistor, and applying a second stored signal to a second output transistor in response to the input signal to change the output signal on the output node, as taught by Chung, to the driver circuit of Itakura, so as to control the slew rate of a driver for reducing power consumption *(Chung: [0090])*.

With respect to **Claim 20**, the method of claim 19, Itakura teaches alternately activating the output transistor and the second output transistor *([0113])*.

Allowable Subject Matter

8. **Claims 3-4 and 10-11** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to **Claims 3 and 10**, none of the prior art teaches a memory includes a memory capacitor and an amplifier, the amplifier being connected to the memory capacitor and

the output transistor such that the amplifier is selectively configured in a voltage follower configuration to store the signal on the control terminal of the output transistor in the memory capacitor.

Response to Arguments

9. Applicant's arguments, see pages 7-10, filed August 16, 2006, with respect to the rejection(s) of claim(s) 9 and 16 under 35 U.S.C 103 (a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Itakura, Mortara and Chung.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
SUPERVISORY PATENT EXAMINER